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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,131	12/16/1999	SARATHY RAJAGOPALAN	65611	8489

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EXAMINER
GUADALUPE, YARITZA

ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 02/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/465,131	Applicant(s) RAJAGOPALAN ET AL.	
	Examiner Yaritza Guadalupe	Art Unit 2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

In response to Request for Continued Examination filed on January 25, 2002.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 - 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art [Hereinafter APA] in view of Nagaraj (US 6,321,175).

APA discloses a thermal profiling device comprising a packaging substrate having an upper surface, and a semiconductor die having an active circuit surface secured directly to the upper surface of the packaging substrate. APA also discloses the semiconductor die including an active circuit surface having conductive bumps and the substrate including a plurality of bonding pads formed on the surface and where the semiconductor die is positioned on the substrate such that the conductive bumps are in electrical contact with the bonding pads. APA discloses the substrate and semiconductor die secured in place by a solder bond between the bumps and the bonding pads, securing the thermocouple in position.

APA does not disclose the thermocouple secured directly to the active circuit surface of the semiconductor die as stated in claim 1.

With respect to claim 1 : APA discloses a flip chip assembly as stated above. Nagaraj discloses a thermal sensing system comprising a thermocouple array / thermal sensor (20) mounted on the bottom side (19) of the printed circuit board / active circuit surface (10) but also gives the option of locating the thermocouple array / thermal sensor array on the top side (18), which is considered to be directly mounted on the active circuit, of the die / printed circuit board (See Column 4, lines 28 – 30) for measuring and controlling the interface temperature between surfaces. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a thermocouple array / thermal sensor secured directly to the active circuit surface of the semiconductor die as taught by Nagaraj in the flip chip assembly disclosed by APA in order to avoid damages due to over heating / over cooling that may affect the overall quality of the circuit.

3. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art [Hereinafter APA] in view of Nagaraj (US 6,321,175) and further in view of Lemoine et al. (US 5,585,577).

APA discloses a device as stated in paragraph 2 above.

APA does not discloses the thermocouple secured directly to the active circuit surface of the semiconductor die, and the opening passing through the second opposite surface and through the first surface of the packaging substrate as stated in claims 6 and 7.

With respect to claim 6 : Nagaraj disclose a system comprising a thermocouple array / thermal sensor as stated above, mounted on the bottom side (19) of the printed circuit board, but also capable of being located in the top side (18) of the printed circuit board / active surface for measuring and controlling the interface temperature between surfaces. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a thermocouple array / thermal sensor secured directly to the active circuit surface as taught by Nagaraj in the flip chip disclosed by APA in order to avoid damages due to over heating / over cooling that may affect the overall quality of the circuit.

Regarding claim 7 : APA and Nagaraj disclose a system as stated above but do not disclose an aperture through the substrate. Lemoine et al. discloses an apparatus having a temperature sensor (32) inserted through a hole / opening (40) in the substrate (10) to locate the sensor directly to a surface / interface to be measured. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an opening through the substrate for inserting the thermocouple to be secured directly to the surface as taught by Lemoine et al. in the device disclosed by APA and Nagaraj since Lemoine is teaching an alternate way to positioned the thermocouple and no reason has been given by APA and

Nagaraj for not doing so, and in order to provide a mechanism to obtain the real temperature of the semiconductor die.

4. Claims 2 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art [Hereinafter APA] in view of Nagaraj (US 6,321,175), as applied to claims 1, 4 and 5 above, and further in view of Hayes (US 5,681,757).

APA and Nagaraj disclose a flip chip assembly as stated in paragraph 2 above.

APA and Nagaraj do not disclose the thermocouple secured using an adhesive comprising epoxy as stated in claims 2 and 3.

Regarding claims 2 and 3 : Hayes discloses a process where an adhesive (44), epoxy (See Column 8, lines 30 – 34), is used on the surface of a substrate (48) for attaching a die (30). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an adhesive as taught by Hayes in the apparatus disclosed by APA and Nagaraj in order to provide a mechanical protection for the thermocouple and provide an electrical conductor as well as a bonding mechanism.

Response to Arguments

5. Applicant's arguments with respect to claims 1 - 6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Burns (US 6,206,267) discloses a device comprising a die / ball grid array (10) to be connected to a substrate, and a thermocouple array (30, 32, 35, 36, 37) connected to the active surface of the die. Capote (US 6,297,560) discloses a flip chip assembly comprising a die / chip (10), and a substrate (20). Bhagath et al. (US 6,229,219) discloses a flip chip package comprising a die (11a), a substrate (15ab), and solder bumps (13). Lewis et al. (US 5,569,950) discloses a device comprising a substrate (14), a die / chip (12), and a thermocouple array (22).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaritza Guadalupe whose telephone number is (703)305 -5676. The examiner can normally be reached on 9:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F.F. Gutierrez can be reached on (703) 308-3875. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Y. Guadalupe
February 7, 2002

DIEGO F.F. GUTIERREZ
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